Specification Amendments

Please replace paragraph 005 with the following rewritten paragraph:

005 As device characteristic dimensions have decreased below about 0.25 microns and lower including less than about 0.17 microns, adequate step coverage of damascene openings with barrier layer deposition methods has become a challenge. Prior art processes have attempted to use various physical vapor deposition (PVD) processes to achieve adequate step coverage. However, ~~PCD~~ PVD processes are inherently limited in depositing thin layers of materials in smaller openings due to the physical nature of sputter deposition processes. For example, PVD processes tend to form a higher coverage at the bottom of the opening compared with the sidewall portions. In addition, with respect to a dual damascene process, barrier layer coverage tends to be thinned at corner portions, e.g., bottom via corner and via/trench transition portions of the dual damascene, making copper diffusion into the IMD layer more likely. In addition, barrier layer coverage over the via bottom portion and sidewall portions in the upper trench portion is generally formed with a relatively increased thickness thereby undesirably increasing electrical resistances.

Please replace paragraph 0014 with the following rewritten paragraph:

0014 Although the present invention is explained by reference to an exemplary dual damascene formation process, it will be appreciated that the method of the present invention applies generally to the formation of damascenes including dual damascenes whereby stacked multi-layer inter-metal dielectric (IMD) layers, also referred to as an inter-layer dielectric (ILD), may be formed with an intervening etch stop layer to improve barrier layer coverage, resistance to copper electro-migration, and improved electrical performance and reliability. Although the method of the present invention is particularly advantageous in forming copper damascenes with characteristic dimensions of less than about 0.17 microns, and aspect ratios (depth to diameter/width) of greater than about 6 to 1, it will be appreciated that the method of the present invention may be adapted to larger characteristic dimension damascene processes.

Please replace paragraph 0015 with the following rewritten paragraph:

0015 By the term damascene is meant any metal filled opening formed in a dielectric insulating layer ~~both~~ e.g., both single and dual damascenes. Further, although the method is particularly applicable and advantageously applied to copper filled damascenes, it will be appreciated that the metal used to fill the damascene opening may include other metals such as tungsten, aluminum, and copper alloys. The

method of the present invention is particularly advantageously used in the formation of copper damascene features such as vias and trench lines with linewidths/diameters less than about 0.25 microns, more preferably less than about 0.17 microns, e.g., 0.13 microns and lower. In addition, the method is particularly advantageously used with silicon oxide based low-K dielectric insulating layers having an interconnecting porous structure and having a dielectric constant of less than about 3.0 including less than about 2.5, for example from about 2.2 to about 3.0. Further, the term 'copper' will be understood to include copper and alloys thereof.

Please replace paragraph 0019 with the following rewritten paragraph:

0019 Still referring to Figure 1A, second etch stop layer 12B is deposited, preferably formed of a composite layer including at least two different material layers, preferably one of the material layers, preferably a lowermost layer, is formed of silicon nitride (e.g., SiN, Si_3N_4) or silicon oxynitride (e.g., SiON), (e.g., SiON) of about 200 to about 400 Angstroms in thickness. Another layer, preferably an uppermost layer, for example an overlying layer, is formed of silicon carbide (e.g., SiC) or silicon oxycarbide (e.g., SiOC) formed at a thickness of about 100 Angstroms to about 300 Angstroms.

Most preferably, the composite etch stop layer 12B is formed of a lowermost layer of silicon nitride and an overlying (uppermost) layer of silicon carbide. The etch stop layer 12B may be formed by conventional CVD processes, for example PECVD or LPCVD. The composite etch stop layer 12B serves to add increased resistance to copper migration and advantageously enables etching endpoint detection using conventional methods, such as optical detection of etching plasma constituents, to enable controlled partial etching through a thickness of the composite etch stop layer 12B as further explained below.